performed using the instruction address to which the address mode information is attached. As a result, it is possible to prevent execution of an instruction fetch with a wrong address mode and to perform branch prediction or recovery from a situation in which a predicted branch address is wrong even when the associated instruction fetch involves changing to another address mode, such as from a 24-bit mode to a 31-bit mode, or vice versa.

**The Prior Art**

**U.S. Patent 5,142,630 to Ishikawa**

The Ishikawa patent is directed to a system for calculating a branch destination address based on as address mode bit in the operand before executing an instruction which changes the address mode and branching. Bit 0 of a general purpose register is used to store a parameter indicating the address mode of the instruction at the destination of a branch instruction and bits 1-31 are used to store parameters required for address calculation to derive the address of the instruction (see column 1, line 47-52; column 3, lines 29-37; and column 4, lines 28-38). As a result, when a branch instruction is decoded, parameters stored at bits 0-31 of the general purpose register are retrieved and the address of the instruction located at the branch destination is derived by a calculation performed according to the specified address mode.

Specifically, as illustrated by Fig. 1 and described at columns 3-4 of Ishikawa, an instruction is fetched from main storage 1 and loaded into instruction register 2. The instruction includes an operation code and pointers to two general purpose registers. The contents of one general purpose register addressed by the instruction is stored in base register 6 and the contents of the other general purpose register are stored in byte index register 7. A selector 11 selects between bit 0 of base register 6 and address mode bit register 4 based on a signal from latch 12 derived from the operation code in instruction register 2 after decoding by decoder 5. Bit 0 in base register 6 may become latched in address mode bit register 4, while bits 1-31 of base register 6 may be used in combination with all of the bits in byte index register 7 to form an operand in operand adder 14. Bit 0 of base register 6 or a previously stored address mode bit in register 4 may be used to adjust the output of operand adder 14 to produce the final operand address stored in register 15.

**U.S. Patent 4,881,170 to Morisada**

The Morisada patent is directed to an instruction prefetch control apparatus using a branch history table. Access to a main memory (MEM) is made in the correct mode by storing both a branch destination address and an associated mode indication in the branch history

table. According to column 4, lines 39-41, the "mode information may include ... a master mode, a privilege mode and a cache bypass mode."

**U.S. Patent 5,963721 to Shiell et al.**

The Shiell et al. patent is directed to a microprocessor system with a capability for asynchronous bus transactions including an out-of-order mode for executing instructions (see column 1, line 41-55 and column 3, line 61 to column 4, line 2).

**In the Drawings**

In paragraph 3 on page 2 of the Office Action, the Examiner objected to the drawings for failure to include a reference numeral. A Letter to the Examiner is submitted herewith requesting approval of the required drawing change. Withdrawal of the objection is requested.

**Rejection under 35 U.S.C. § 102(b)**

In paragraphs 6-17 on pages 2-7 of the Office Action, the Examiner rejected claim 1-3, 5, 6, 8-10 and 12-15 under 35 U.S.C. § 102(b) as anticipated by Ishikawa. At the top of page 3 of the Office Action in sub-item a, it was asserted that column 1, lines 43-52 disclosed the storage circuit recited as the first element of claim 1. As described at column 4, line 10-38, when a BSM or BASSM instruction is decoded in the preexecution cycle, the address mode signal corresponds to bit 0 of base register 6 and if the address mode signal is a 1, bit 0 of operand address register 15 is set to 0 and bits 1-31 of operand register 15 are set to bits 1-31 of base register 6. Thus, in this specific instance the base register 6 might correspond to storage circuit 6 as recited in claim 1. However, it is implied by Ishikawa that if the BSM or BASSM instruction is not decoded in the preexecution cycle, the address mode signal will be obtained from address mode bit register 4, not base register 6 and if bit 0 of base register 6 is 0 when a BSM or BASSM instruction has been decoded in the preexecution cycle, only bits 8-13 of base register 6 are used for the instruction address. In this case, the contents of bits 1-31 in base register 6 will not correspond to the instruction address of the instruction to be fetched.

Furthermore, it is submitted that Ishikawa does not disclose "a branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction" (claim 1, lines 4-5). The only use of address mode information disclosed in Ishikawa is in address adjuster 13. The address adjuster is not described by Ishikawa as having anything to do with how a branch instruction is executed.

In addition, the components responsible for transferring the address mode information to address adjuster 13 operate "[W]hen the BSM instruction or the BASSM instruction is decoded by the decoder 5 **in the preexecution cycle**" (column 4, line 10-11, emphasis added), not "when the branch instruction **is executed**" (claim 1, last line, emphasis added). Therefore, there is nothing that corresponds to either the branch instruction control circuit or the transfer circuit that performs the operations recited for these elements of claim 1. For the above reasons, it is submitted that claim 1 patentably distinguishes over Ishikawa. Since claims 2, 3, 5, 6 and 8 depend from claim 1, it is submitted that claims 2, 3, 5, 6 and 8 patentably distinguish over Ishikawa for the reasons set forth above.

Claim 9 recites the same limitations as claim 1, except that the word "address" does not precede the words "mode information". Nothing has been cited or found in Ishikawa which would make this difference result in claim 9 being anticipated by Ishikawa. Therefore, it is submitted that claim 9 distinguishes over Ishikawa for the reasons discussed above with respect to claim 1.

Claims 13 and 14 recite combinations of means-plus-function elements that perform functions recited using the same language as the elements recited in claims 1 and 9, respectively. Therefore, it is submitted that claims 13 and 14 patentably distinguish over Ishikawa for the reasons discussed above with respect to claims 1 and 9, respectively.

Claim 10 recites "a storage circuit storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction" (claim 10, line 3-5). As discussed above with respect to claim 1, the general purpose registers 3 do not store "mode information of **each** fetched instruction as part of an instruction address" (claim 10, lines 3-5, emphasis added), but only for instructions that are fetched when a BSM or BASSM instruction is decoded in the preexecution cycle. The portion of column 1 cited in sub-item b near the top of page 5 of the Office Action confirms that the description is applicable "when an operation code indicated the BSM instruction code" (column 1, lines 43-44). Therefore, it is submitted that claim 10 and claim 15 which recites similar limitations in a means-plus-function element, patentably distinguish over Ishikawa.

Claim 12 has been amended to recite "storing mode information of the fetched instruction as part of an instruction address of the fetched instruction in each cycle of an instruction process for the fetched instruction" (claim 12, lines 5-7). The same portion of column 1 of Ishikawa discussed above with respect to claim 10 was cited as teaching the step of storing mode information as recited in claim 12. However, nothing in this portion of Ishikawa

or anything else that has been found in Ishikawa discusses "storing mode information of the fetched instruction" (claim 12, line 5), let alone storing it "as part of an instruction address of the fetched instruction" (claim 12, lines 5-6) or anything that occurs "in each cycle of an instruction process" (claim 12, line 6). Therefore, it is submitted that claim 12 patentably distinguishes over Ishikawa for the reasons set forth above.

**Rejections under 35 U.S.C. § 103**

In paragraphs 19-21 on pages 7-8 of the Office Action claims 4 and 7 were rejected under 35 U.S.C. § 103(a) over Ishikawa in view of Morisada. In paragraph 20 on page 7 of the Office Action, it was acknowledged that Ishikawa did not teach a branch instruction control circuit which "judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction are correct using the address mode information and instruction address of the branch destination" (claim 4, lines 3-7). Therefore, Morisada was cited as providing this teaching and as obvious to combine it with the teachings in Ishikawa.

As discussed above, the mode indicator taught by Morisada relates to "a master mode, a privilege mode and a cache bypass mode" (column 4, lines 39-41) none of which appear to relate to "**address** mode information" (claim 4, line 3, emphasis added). While Morisada might suggest the value of adding branch history storage to Ishikawa, it is submitted that the combination of these two references would not suggest using such a branch history storage to store address mode information as recited in claim 4. Nor would the addition of Morisada overcome the deficiencies of Ishikawa discussed above with respect to claim 1 from which claim 4 depends. For the above reasons, it is submitted that claim 4 patentably distinguishes over Ishikawa in view of Morisada.

Claim 7 is similar to claim 4 in that it recites "storing ... address mode information and instruction addresses" (claim 7, lines 6-8), although in the case of claim 7, the address mode information and instruction addresses are "of the branch instruction and branch destination" (claim 7, lines 8-9). As discussed above with respect to claim 4, Morisada does not teach or suggest storing address mode information and does not overcome the deficiencies of Ishikawa discussed above with respect to claim 1. Therefore, it is submitted that claim 7 similarly distinguishes over the combination of Ishikawa and Morisada.

In paragraphs 22-26 on pages 9-10 of the Office Action, claims 11 and 16 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ishikawa in view of Shiell et al. In paragraph 24, it was acknowledged that Ishikawa does not disclose a "device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system"

(claim 11, lines 1-2), but Shiell et al. was cited as disclosing both operations at column 1, lines 41-55 and Figs. 1 and 2. However, nothing has been cited or found in Shiell et al. that overcomes the previously noted deficiency of Ishikawa to teach or suggest "storing a plurality of combinations of mode information of an instruction to be fetched and an instruction address of the instruction" (claim 11, lines 4-5). Therefore, it is submitted that claim 11 and claim 16 which has been similarly amended to recite the quoted limitation as being performed by a means-plus-function element, patentably distinguish over Ishikawa in view of Shiell et al.

**New Claim 17**

Claim 17 has been added to recite limitations similar to those discussed above with respect to claims 1 and 11. As a result, none of the elements recited in claim 17 can be found in Ishikawa taken alone or when combined with any of the other cited references.

**Summary**

It is submitted that the cited references, taken individually or in combination, do not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-17 are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If any further fees are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from Deposit Account Number 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 3/18/03

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CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on 3/18, 20 03

STAAS & HALSEY

By: [signature]

Date: 3/18/03

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE SPECIFICATION:**

Please REPLACE the paragraph beginning at page 4, line 11, with the following paragraph:

According to the conventional instruction processing device, since an address mode indicating the bit size of an address space is determined by software, the address mode is sometimes changed while an instruction is executed. However, when the branch prediction of a branch instruction accompanied by an address mode change is made, only the instruction address of a branch destination can be predicted since a mechanism for predicting the address mode of a branch destination is not provided. Therefore, the pre-fetch of a branch destination instruction string cannot be performed based on the changed address mode, and thereby a correct instruction process cannot be executed.

**IN THE CLAIMS:**

Please AMEND the claims according to the following:

1. (ONCE AMENDED) An instruction processing device, comprising:

a storage circuit storing a combination of address mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

a branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

2. (ONCE AMENDED) The instruction processing device according to claim 1, wherein said branch instruction control circuit stores a combination of address mode information of a branch destination of the branch instruction [with] and an instruction address of the branch destination.

9. (ONCE AMENDED) An instruction processing device, comprising:

a storage circuit storing a combination of mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

a branch instruction control circuit controlling a branch instruction using the mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

11. (ONCE AMENDED) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

a storage circuit storing a plurality of combinations of mode information [obtained when] of an instruction [fetch request is issued, with] to be fetched and an instruction address [for each port] of the instruction, each combination related to each of the plurality of instruction fetch ports; and

a fetch circuit performing an instruction fetch based on mode information corresponding to a port to be used.

12. (ONCE AMENDED) An instruction processing method, comprising:

handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as a part of an instruction address;

fetching an instruction;

storing mode information of the fetched instruction as a part of an instruction address of the fetched instruction in each cycle of an instruction process for the fetched instruction; and

controlling the instruction process for the fetched instruction based on the stored mode information.

13. (ONCE AMENDED) An instruction processing device, comprising:

storage means for storing a combination of address mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the address mode information stored in the storage means to the branch instruction control means when the branch instruction is executed.

14. (ONCE AMENDED) An instruction processing device, comprising:

storage means for storing a combination of mode information of a fetched instruction [with] and an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction is executed.

16. (ONCE AMENDED) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

storage means for storing a plurality of combinations of mode information [obtained when] of an instruction [fetch request is issued, with] to be fetched and an instruction address [for each port] of the instruction, each combination related to each of the plurality of instruction fetch ports; and

fetch means for performing an instruction fetch based on mode information corresponding to a port to be used.

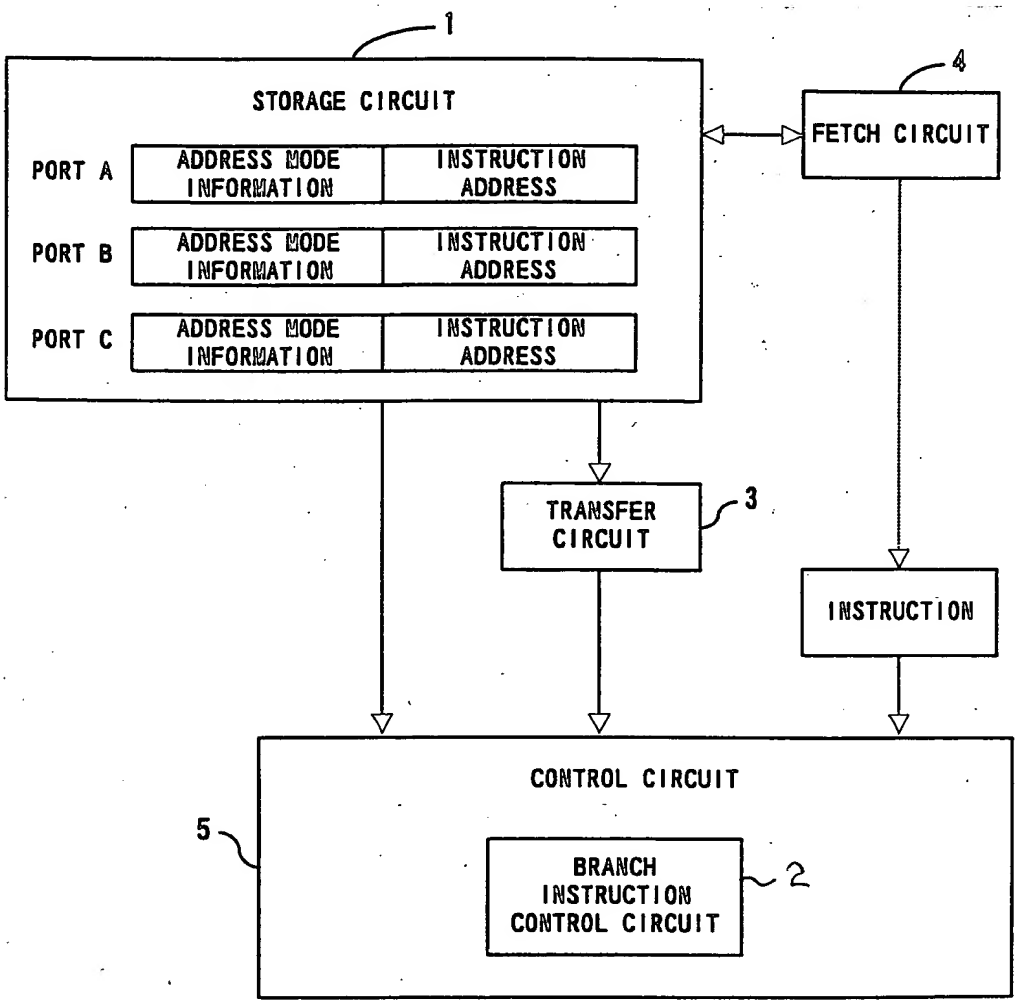


FIG. 1